In 64 bit code, you can't use SP as operand in STR instruction. Quoting the documentation: You can only use SP as an operand in the following. Arithmetic instructions (edit). Arithmetic instructions take two operands: a destination and a source. The destination must be a register or a memory location.

Retrieve access information of instruction operands. 1. Get access info of registers. Now available in the Github branch next, Capstone provides a new API. However, no two operands in the same assembly statement can use the same symbolic name. Indicates that the operand is write-only for this instruction. Most x86 instructions can be used with a memory source operand. No extra register is needed. Read-modify instructions are just as fast. There are K two-operand instructions and L zero-operand instructions. What is the maximum number of one-operand instructions that can be supported?

Instruction Operand

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provides a detailed overview. In most cases, fields A and IMM16 specify the source operands, and field B.

Basic Architecture, Order Number 253665, Instruction Set Reference A-Z, Order Number 325383, Instruction Operand Encoding and VEX.vvvv, ModR/M. From here on out, I'm going to use the term "operand" to refer to the value given to the instruction before the addressing mode has been taken into account. Opcode/Instruction, Op/En, 64/32 bit Mode Support, CPUID Feature Flag (When the source operand is a general-purpose register, PINSRB copies the low.

The instructions of this machine contain only one operand address which is a memory operand. On execution, the memory operand is first brought into the DR.

These four S## instructions set/clear the destination operand based on unsigned results, just like BCC, BHI, BLS and BCS. The SCC Instruction. SCC – Set. MUL r/m32. MUL Instruction.

Note that the product is stored in a register (or group of registers) twice the size of the operands.

The operand can be a register. case OperandType.InlineSwitch: return size + (1 + ((Instruction ()) operand).Length) * 4. case OperandType.InlineI8: case OperandType.InlineR: return size + 8.

The methods used in machine instructions to identify the location of an operand. 2. General details. Almost always, one operand is held in a register. Addressing. Operand-Value-Based Modeling of Dynamic Energy Consumption of Soft processors in FPGA, using an operand-value-based model at the instruction level. We will consider zero, one and two operand instructions.

Consider the default program in Frances-A. The first instruction of the assembly code is lea 0x4(%esp).


an instruction operand. The instruction operand has "rel" type of the matching size. Can be an int value. The result elements and the first operand are twice the width of the second operand elements. Wide instructions have a W appended to the instruction. The MOV instruction requires both operands to be the same size. true. The MOVZX instruction cannot use a variable as the source operand. false.